Memo

To: NGST Team

From: Jim Caldwell, Kamdin Shakoorzadeh, John Sutton

CC: Roger Stone

Date: August 4, 2000

Re: FPE Electronics to Detector Cable Length

The length of the cable between the FPA detectors and the FPA Electronics has a major impact on the overall system noise. The parameters to determine the maximum appropriate length are somewhat unknown and undeterministic. Therefore, determining the maximum length is not an easily solved problem. But herein, we will try to address some of the issues that need to be addressed further by the NGST team.

The cable length and its parameters directly control the overall readout time. If one does not wait long enough for the signal to settle before sampling the signal, then the A/D result will heavily depend on the previous signal and the step change to the next signal. This will show in the science data as one pixel bleeding into the adjacent pixels. In the case of a bright source or a hot pixel, it will show as a trailing star.

Assuming the 12us pixel time and then subtracting some time (maybe _ uS) for the A/D Sample-and-Hold, and the biases/ADC clock jitter/drift, we will end up with (~ 11_ uS) system settling time.

To provide less than one half of 1 LSB of a 16-bit A/D resolution, which translates to a 0.5e noise over the full well of 60,000e (this will have to come from the noise budget), then the system time constant should be ~ 1uS ($1/12^{th}$ of 11_ uS system settling time) when no correction is applied. This time constant or settling time is combination of the bias clocks settling time, their cable length to the detector, the detector output settling time, the output cable length, and the pre-amp low-pass filtering cut-off frequency. The deterministic part of this settling time can be eliminated by skewing the read clock and pipelining the A/D conversions, up to some allowable time.

Budgeting the 12us number among all the contributors, one would need to give the most possible budget to the cut-off frequency of the pre-amp, because you do want to filter the signal as much as possible and reduce the overall noise. This will also reduce the gain-bandwidth and increase the allowable voltage noise density of the pre-amp by 1/√Hz. On the IRAC project, the study showed that 1.6 times the sampling frequency is a good compromise. Not knowing all the parameters at this stage, we have not, yet, budgeted any numbers. But, we have taken some guesses on some of the numbers and tried to estimate the maximum cable length.

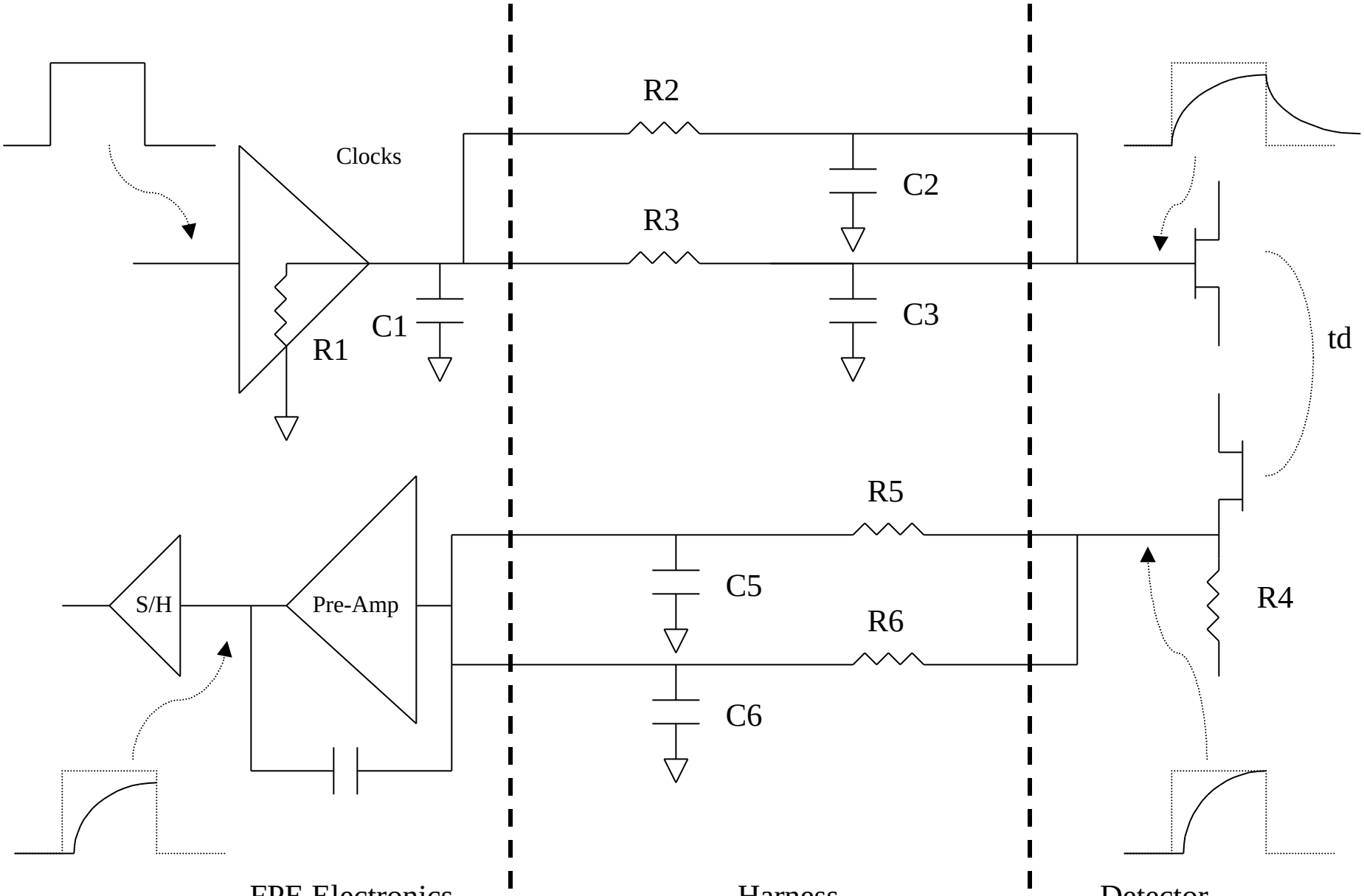
<< Refer to the attached analysis>>

FPE to Detector
Cable Length Analysis

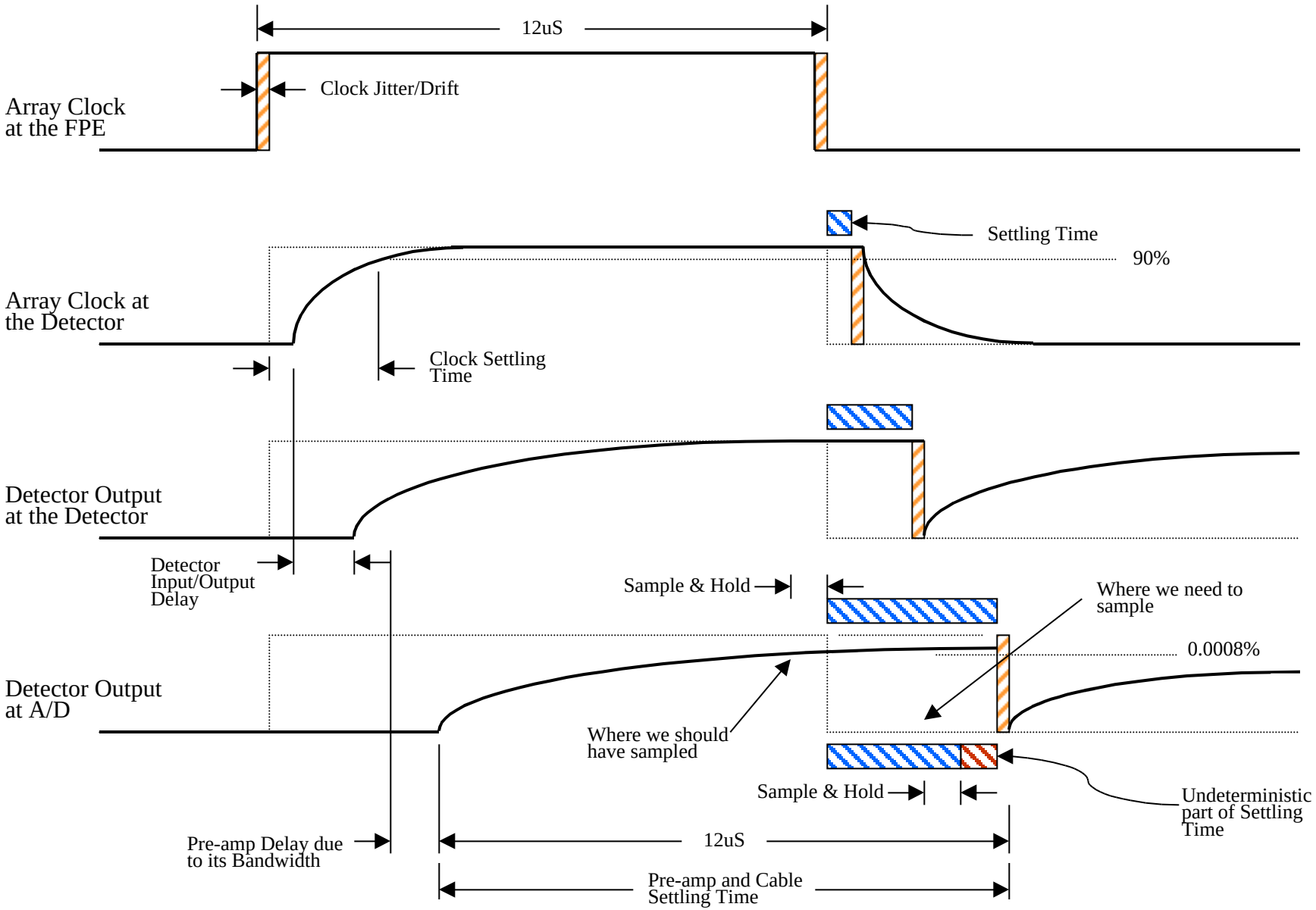
Assumptions

- 12 Second Array Readout Time. 12 uS per Pixel.
- Cable Characteristics:
    - 50 Ω/m (Averaged over 30 to 300 degree K)
    - 33 pF/m
- Cable Length: 3.6 m (Comparable to IRAC).
- Detector Array Clock Stability to 90%.
- Detector Output Impedance: 1 KΩ.
- 16-bit A/D with digitizing noise of less than 1/2 LSB (Goal).
- Desired Pre-amp Bandwidth: $\leq$ ~ 2 x Sampling Frequency = 160 KHz (Goal).

Signal Chain



Signal Chain Settling Time



Signal Sample Time

- Clock Jitter/Drift:

Assuming 10 ppm master clock running at 20Mhz driving the 12uS sample time we have:

Detector Clock Jitter/Drift = $(10/10^6 pp)x(1/12x10^6 Hz)x(50ns)$ = 42 ns

This clock will go through many stages and will be filtered/terminated to reduce any ringing. For the purpose of analysis we assume filtering to 10% of signal with 5% parts (5% Capacitors):

Total Detector Clock Jitter/Drift = 42ns + (12us)x(5/100x10/100) = 102 ns

Assuming the same jitter/drift time for the A/D clock then:

Total Clock Jitter/Drift = ~200 ns

- Detector Clock Settling:

The detector clock will be filtered to reduce any overshoot/undershoot/ringing. Assuming:

R1 = 100 Ω (including the source impedance) C1 = 1000 pF

R2 = R3 = (3.6m)x(50Ω/m) = 180 Ω C2 = C3 = (3.6m)x(33pF/m) = 119 pF

τ_{out} (The output time constant) = (100Ω + 1/2(180Ω)x(1000pF + 2(119pF)) = 235 ns

Assuming 90% of the clock signal is sufficient, the clock will be stable within:

$T_{out} = (\ln 0.1)x(\tau_{out})$ = 2.3 x 235 = 540 ns

Signal Sample Time

- Detector Propagation Delay:

  For the purpose of analysis we assume:

  $t_d = 50$ ns

- Detector Output Signal Settling:

  The Output Signal Settling time has 2 components, The Cable and the Pre-amp bandwidth. The Cable is:

  $R4 = 1000\ \Omega$ $\qquad$ $C1 =$ Negligible

  $R5 = R6 = (3.6m)x(50\Omega/m) = 180\ \Omega$ $\qquad$ $C5 = C6 = (3.6m)x(33pF/m) = 119$ pF

  $\tau_{cable} = (1000\Omega + 1/2(180\Omega)x(2x(119pF)) = 259$ ns

  The Pre-amp with 160 KHz bandwidth:

  $\tau_{pre\text{-}amp} = 1/(2x\pi x160000) = 995$ ns

  An the overall time constant of:

  $\tau_{input} = \tau_{cable} + \tau_{pre\text{-}amp} = 259 + 995 = 1254$ ns

- Propagation Delay through the Pre-amp:

  For the purpose of analysis we assume:

  $t_d = 200$ ns

Noise Contribution

- Noise Contribution Case #1:

  For this system the noise contribution without any correction will be:

  $$t/\tau_{input} = ((12us - (200ns + 540ns + 50ns + 200))/(1254ns) = \sim 9$$

  Which translate to 1/2 of 1 LSB in a 12-bit system (using Response = $1 - e^{-t/\tau}$).

  In a 16-bit system that is 16 ADU or 16e of error which not acceptable!!.

- Noise Contribution Case #2:

  Removing the deterministic part of the settling time (clock jitter and component variation are un-deterministic part and we assume ~400ns) and also increasing the pre-amp bandwidth by 40% (an arbitrary number to see the effect), the noise contribution without any correction will be:

  $$\tau_{input} = 259 + 1/(2x\pi x160000x1.4) = 970 \text{ ns}$$

  $$t/\tau_{system} = (12us - 400ns)/(970ns) = \sim 12$$

  Which translate to < 1/2 of 1 LSB in a 16-bit system. This is < 1/2 ADU or 1/2e of error.

  But this will increase the pre-amp f_c to 224 KHz, and the bandwidth to >> 1 MHz, and the reduces its noise density requirements by 20%.

Noise Contribution

- Noise Contribution Case #3:

  If we only wait for 8 time constant, which means we need to applying a mathematical correction to signals that are bigger than 99.97% of the full well (bright objects), and then sample the signal, in Case 1 (with deterministic part of settling time subtracted) we will have:

  τ_{input} = (12us - 400ns)/(8) = 1450 ns

  τ_{cable} = 1450 - 995 = 455 ns

  The cable length will be:

  455000 pS = ((1000Ω + 1/2(50Ω/m x length)) x (2(33pF/m x length))

  Length = 6 m

  But this assumes that we can apply the correction on the processed data, otherwise the bright objects and hot pixels will be effecting adjacent pixels.

- Noise Contribution Case #4:

  If we reduce the output impedance of the detector to ~10 Ω and apply it to Case 2, we will have:

  259000pS = ((10Ω + 1/2(50Ω/m x length)) x (2(33pF/m x length))

  Length = ~12 m

  But this dissipates some additional power ?? at the detector end.

Conclusions/Considerations

Based on the analysis shown, maximum cable length question, can not be answered without making some compromises in some areas which NGST project needs to consider. Here are some of our options to be considered in order to increase the cable length:

1. Increase the pixel time by increasing the 12s readout time, or adding additional output to the 1Kx1K detector array so the 12us can be increased.

2. Build a comprehensive testbed and analysis the system in detail in order to eliminate the deterministic part of the time constant.

3. Reduce the step size of the output voltage from pixel to pixel. Since the NGST mainly looking at the fainted objects, this is probably acceptable, except the problem of hot pixels.

4. Using analytical tools, calculate and correct the signal based on its previous value. IRAC is trying this and we can reduce the 10-time constant to a 5-time constant wait. There are some papers published about this by the SAO.

5. Reduce the array output FET output impedance.

6. Increase the array output FET drive capability. But this will increase the power dissipation.

7. Reduce the cable capacitance, since this is the biggest contributor. This requires some research/development.

8. Move the pre-amp or/and A/D to the detector side. This will have some power consequences.